Description

PPM RECEIVING SYSTEM AND METHOD USING TIME-INTERLEAVED INTEGRATORS

BACKGROUND OF INVENTION

[0001]   The present invention relates generally to high data rate communication systems. More particularly, the present invention is related to a system and method of extracting information from pulse-position modulated (PPM) signals.

[0002]   Existing high data rate optical networks, such as the Internet backbone networks embody OC-192 or OC-768 standards, which have data transfer rates of 10Gbit/s and 40Gbits/sec, respectively. The existing networks typically rely upon a clock and a data recovery scheme that utilizes amplitude modulation (AM).

[0003]   The available signal-to-noise ratios and the lengthy transmission distances involved within these systems have limited the modulation formats and have necessitated a high degree of error-correction coding overhead. The

modulation has been limited to one bit per symbol ON-OFF keying. The error-correction coding overhead allows for the bit-error rates that are required of the Internet networks.

[0004] The general approach to obtaining the higher data rates in Internet networks and the like has been to increase the clock rate and to focus engineering attention on solving the problems associated with the transmitting and receiving of ever-higher bandwidths, which are associated with higher data rates. In general, even without transmitting and receiving at high data rates, AM systems are sensitive to attenuation and amplitude type noise, which degrades the signal-to-noise ratio. The AM systems also tend to exhibit power and signal losses. In AM systems when data rates are increased noise sensitivity and signal losses tend to increase. Signal losses can include dielectric loss and skin-effect loss, as well as loss from connectors, line impedance mismatches, series capacitors, passive equalizers and pulse shaping, and differential and signal ended transmissions, or signal transmissions.

[0005] Some other available communication systems incorporate the use of pulse-position modulation (PPM) for the transmission and reception of data. PPM does not exhibit the

same noise and signal losses as that of AM type systems. Since signals are modulated in time, the signals are less sensitive to amplitude noise and power losses. However, PPM systems are constrained by receiver accuracy to significantly lower data rates. Current PPM systems monitor positions of pulses within time slots. As data rates increase, width of the time slots decreases, resulting in the need for a more accurate receiver.

[0006] Several PPM type communication systems do exist that are capable of receiving the high data rates, but unfortunately these systems rely upon optical techniques that require hardware that is complex, costly, and of a large physical form factor.

[0007] Thus, there exists a need for an improved PPM receiver and method of extracting information from PPM signals that supports high data rates, has high signal-to-noise performance, is robust, simple, inexpensive, and has reduced form factor size.

SUMMARY OF INVENTION

[0008] The present invention provides a communication system and method of extracting information from pulse-position modulated (PPM) signals. A communication receiver is provided and includes a data receiver that receives a

pulse-position modulated signal. A clock circuit separates a reference clock signal into multiple coordinating clock signals. Multiple time integrators are gated to generate multiple time-integrated signals in response to the pulse-position modulated signal and the coordinating clock signals. A combiner forms a demodulated signal from the time-integrated signals.

[0009] The embodiments of the present invention provide several advantages. One such advantage that is provided by several embodiments of the present invention is the provision of a PPM receiver that incorporates the use of time-interleaving integrators and analog signal processing. In so doing, the stated embodiments provide a robust PPM receiver with increased data rate reception capability and improved timing accuracy. In being more accurate, the stated embodiments provide improved resolution and thus improved signal-to-noise performance.

[0010] Another advantage that is provided by multiple embodiments of the present invention is the provision of parallel processing time-interleaved integrated signals within a PPM receiver. The parallel processing allows for increased bit or data rates with minimal time allotted for resetting of components.

[0011] Furthermore, the present invention provides a PPM receiver that is simple, inexpensive, and has reduced form factor size.

[0012] Moreover, the multiple embodiments of the present invention provide versatility in the ability to be utilized in various applications.

[0013] The present invention itself, together with further objects and attendant advantages, will be best understood by reference to the following detailed description, taken in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF DRAWINGS

[0014] Figure 1 is a block diagrammatic view of a communication system utilizing pulse position modulation (PPM) receivers in accordance with an embodiment of the present invention;

[0015] Figure 2 is a schematic and block diagrammatic view of a PPM receiver in accordance with an embodiment of the present invention;

[0016] Figure 3 is a timing diagram for signal outputs of a clock circuit and an integrator circuit of the PPM receiver of Figure 2 and output of the PPM receiver in accordance with an embodiment of the present invention;

[0017] Figure 4 is a simplified schematic diagram of a sample in-

tegrator that may be utilized within the PPM receiver in accordance with an embodiment of the present invention;

[0018] Figure 5 is a detailed schematic diagram of a sample integrator that correlates with the schematic of the integrator of Figure 4 in accordance with an embodiment of the present invention; and

[0019] Figure 6 is a logic flow diagram illustrating a method of extracting information from pulse position modulation signals in accordance with multiple embodiments of the present invention.

DETAILED DESCRIPTION

[0020] While the present invention is described with respect to a system and method of extracting information from pulse position modulation (PPM) signals, the present invention may be adapted to be used in various applications known in the art. The present invention may be applied to various communication systems, broadband systems, Internet based systems, satellite systems, telecommunication systems, optical communication systems, fiber optic systems, and network systems, as well as other communication systems known in the art. The present invention may be applied to communication systems that utilize pulse position modulation and to communication systems that uti-

lize other time modulation techniques.

[0021] In the following description, various operating parameters and components are described for one constructed embodiment. These specific parameters and components are included as examples and are not meant to be limiting.

[0022] Referring now to Figure 1, a block diagrammatic view of a communication system 10 utilizing PPM receivers 12 in accordance with an embodiment of the present invention is shown. The communication system 10 includes a central station 14 that is in communication with multiple remote stations 16 via fiber optic cable 18. The central station 14 is coupled to and provides access to the Internet 20 for the remote stations 16. The central station 14 and the remote stations 16 include the PPM receivers 12 and PPM transmitters 22 for receiving and transmitting communication signals therebetween. The receivers 12 and transmitters 22 are coupled to the fiber optic cable 18 via optic couplers 24. The receivers 12 and transmitters 22 are capable of supporting high data rate communication. High data rate communication refers to data rates of at least approximately 10 Gbits/s. The communication signals may include clock signals, data signals, pulse modulation signals, and other communication signals known in

the art.

[0023] Referring now to Figure 2, a schematic and block dia-grammatic view of a PPM receiver 30 in accordance with an embodiment of the present invention is shown. The re-ceiver 30 includes a clock receiver 32 and a data receiver 34 that receive reference clock signal(s) 36 and data sig-nal(s) 38, respectively. The clock receiver 32 and the data receiver 34 may be in the form of photodiodes or some other electrical transducer known in the art. The clock signals 36 and the data signals 38 may be in the form of current signals, depending upon the receivers 32 and 34. In the embodiment as described, the data signal 38 is in the form of a PPM signal. The clock receiver 32 is coupled to a first transimpedance amplifier 40 and the data re-ceiver 34 is coupled to a second transimpedance amplifier 42. The amplifiers 40 and 42 convert the clock signal 36 and the data signal 38 into voltage swing type signals for analog processing thereof. The clock signal 36 may be re-ceived separately from the data signal 38, as shown, or for some coding schemes maybe recovered from the data signal 38.

[0024] The first amplifier 40 has a first amplifier input 46 and a first amplifier output 48. The second amplifier 42 has a

second amplifier input 50 and a second amplifier output 52. The first amplifier input 46 is coupled to the clock receiver 32 and the second amplifier input 50 is coupled to the data receiver 34. The first amplifier output 48 is coupled to a first one-shot timer circuit 54 and the second amplifier output 52 is coupled to a second one-shot timer circuit 56. The timer circuits 54 and 56 widen pulses within the clock signal 36 and the data signal 38. The widened clock signal is referred to as an electrical clock signal E_{clk} and the widened data signal is referred to as an electrical data signal E_{data}. The amplifiers 40 and 42 may have reference terminals 58.

[0025] A clock recovery circuit 44 may be used instead of the clock receiver 32 and the amplifier 40 to recover the clock signal 36 from the data signal 38. The clock recovery circuit 44 may be coupled between the second amplifier output 52 and the first timer circuit input 60, as shown, between the second amplifier input 50 and the first amplifier input 46, or elsewhere as known in the art. The clock recovery circuit 44 may be in the form of a phase lock loop or in some other form known in the art.

[0026] The first timer circuit 54 has a first timer input 60 and a first timer output 62 and the second timer circuit 56 has a

second timer input 64 and a second timer output 66. The first circuit output 62 is coupled to a clock circuit input 68 of a coordinating clock circuit 70 that has multiple clock circuit outputs 72. The clock circuit 70 separates the electrical clock signal E_{clk} into multiple coordinating clock signals 74 having different phase. The clock circuit 70 may be in the form of a three-phase clock generator, as shown, or may be in some other form known in the art. The clock circuit 70 has the three outputs 72, which have coordinating clock signals A, B, and C, respectively. The clock circuit 70, although shown having a specific number of inputs and outputs, may include any number thereof.

[0027] A time-interleaving integrator circuit 76 is coupled to the clock circuit 70 and to the second timer circuit 56. The integrator circuit 76 provides an analog representation of the electrical data signal E_{data} through the use of time-interleaving signal processing. The integrator circuit 76 includes multiple phase integrators 78. Each integrator 78 includes an integrator input 80, a hold input 82, a reset terminal 84, and an output 86. The integrator inputs 80 and the reset terminals 84 are coupled to the clock circuit outputs 72. Each of the hold inputs 82 are coupled to the second timer circuit output 66. The outputs 86 are cou-

pled to the switches 88. The integrators 78 have analog output signals IntA, IntB, and IntC, respectively. Each integrator 78 may operate in an integration mode, a hold mode, or a reset mode, as is described in further detail below.

[0028] Each of the switches 88 has a switch input 90, a control terminal 92, and switch output 94. The switch inputs 90 are coupled to associated integrator outputs 86. The control terminals 92 are coupled to associated clock circuit outputs 72. The switch outputs 94 are coupled to a combiner 96, which sums the analog output of each switch 88 to form a resulting demodulated signal V_{dem}. The resulting signal V_{dem} may be read at the output terminal 98.

[0029] In the embodiment as shown, the clock circuit 70 includes a first output 100, a second output 102, and a third output 104. The integrator circuit 76 includes a first phase integrator 106, a second phase integrator 108, and a third phase integrator 110. The switches 88 include a first switch 112, a second switch 114, and a third switch 116. The first output 100 is coupled to the second reset terminal 118, of the second integrator 108, and to the third control terminal 120, of the third switch 116. The second output 102 is coupled to the third reset 122, of the third

integrator 110, and to the first control terminal 124, of the first switch 112. The third output 104 is coupled to the first reset 126, of the first integrator 106, and to the second control terminal 128, of the second switch 114.

[0030] Referring now also to Figure 3, a signal timing diagram for the clock circuit 70 the integrator circuit 76, and the receiver 30 of Figure 2 in accordance with an embodiment of the present invention is shown. The timing diagram illustrates the relation between the electrical clock signal E_{clk}, the electrical data signal E_{data}, the coordinating clock signals A, B, and C of the integrators 78, the analog output signals IntA, IntB, and IntC, and the resulting signal V_{dem}. Each of the stated signals is shown as a respective voltage amplitude representation over time.

[0031] In operation, each symbol within the electrical data signal E_{data} is encoded as the time delay between the rising edge of a pulse of the electrical clock signal E_{clk} and the rising edge of a subsequent pulse of the electrical data signal E_{data}. Three sample time delays are shown and represented by

$$\tau_n, \tau_{n+1}, \text{ and } \tau_{n+2}$$

. Pulses 150 of the electrical clock signal E_{clk} trigger states

of the clock circuit 70. The clock circuit 70 has three states to produce the coordinating clock signals A, B, and C.

[0032] In the first state, corresponding to a first clock pulse 152, the first integrator 106 commences integration with the rising edge 154 of the coordinating signal A and proceeds until switched into a hold mode by the rising edge 156 of the following or first data pulse 158. The integration is represented by the first ramp 160 having a fixed slope of the first analog output signal IntA. The first integrator 106 integrates at a constant rate over the time delay

$$\tau_n$$

such that the first ramp 160 has an approximately fixed slope. By integrating with a constant rate, the time delay

$$\tau_n$$

is linearly converted to a voltage representation. The first integrator 106 integrates until the rising edge 156 of the first data pulse 158 and then operates in the hold mode. With the rising edge 154, the second integrator 108 operates in the reset mode and the third switch 116 is closed. The second integrator 108 is reset to an initial condition

or low state in response to the rising edge 154 of the co-ordinating signal A. The third integrator 110 operates in a hold mode as a result of a prior data pulse (not shown). Since the third switch 116 is in a closed state and the first switch 112 and the second switch 114 are in an open state, the resulting signal V_{dem} is approximately set equal to the voltage of the third analog output signal IntC. Timing stages of the resulting signal V_{dem} are represented by V_{n-1}, V_n, and V_{n+1}.

[0033] In the second state, corresponding to a second clock pulse 162, the first integrator 106 is in the hold mode, the second integrator 108 commences integration, and the third integrator 110 is in the reset mode. The first integrator 106 is in a hold mode due to the rising edge 156. The second integrator 108 commences integration with the rising edge 164 of the coordinating pulse B to convert the time delay

$$V_{n+1}$$

into a voltage equivalent representation. The second integrator 108 operates in the integration mode until a rising edge 166 of the second data pulse 167. The rising edge 164 resets the third integrator 110. The first switch 112 is

closed with the rising edge 164. The second switch 114 remains open whereas the third switch 116 is switched open in response to the falling edge 168 of the coordinating signal A. The resulting signal V_{dem} is set approximately equal to the voltage of the first analog output signal IntA.

[0034] In the third state, corresponding to a third clock pulse 170, the first integrator 106 is reset, the second integrator 108 operates in the hold mode, and the third integrator 110 operates in the integration mode. The rising edge 172 of the coordinating signal C resets the first integrator 106. The second integrator 108 operates in the hold mode in response to the rising edge 166. The third integrator 110 operates in the integration mode in response to the rising edge 174 of the third clock pulse 170 and integrates until a rising edge 176 of the third data pulse 178. The first switch 112 is opened, the second switch 114 is closed, and the third switch 116 remains open. The resulting signal V_{dem} is set approximately equal to the voltage of the second analog output signal IntB.

[0035] Thus, in turn, each of the three-phase integrators 78 1) integrate a data symbol (coded as a time delay), 2) hold the corresponding voltage of the data symbol for detec-

tion, and 3) are reset to an initial state from which integration can begin again. The time-interleaving design of the receiver 30 allows for a full clock cycle to be allotted for both reading the output voltage of the receiver 30 and for resetting each integrator 78, which alleviates the time constraints imposed by high clock frequencies.

[0036] Referring now to Figure 4, a simplified schematic diagram of a sample integrator 200 that may be utilized within a PPM receiver in accordance with an embodiment of the present invention is shown. The integrator 200 includes three switches 202 and a current source 204. An integration switch 206 is coupled between and in series with a first capacitor 208 and the current source 204. The capacitor 208 has a positive terminal 210 and a negative terminal 212. The positive terminal 210 is coupled to a ground 214 and the negative terminal 212 is coupled to an output terminal 216. The integration switch 206 has a first integration leg 218, an integration control leg 220, and a second integration leg 222. The first leg 218 is coupled to the output terminal 216. The control leg 220 is coupled, for example, to the output of a set/reset latch (not shown), which may be included within the integrator 200. The set and reset inputs of the set/reset switch are

coupled to the coordinating clock circuit outputs 72 and to the second timer output 66, respectively. The second leg 222 is coupled to the current source 204, which is in turn coupled to a voltage source 224.

[0037] A reset switch 226, having a first reset leg 228, a reset control leg 230, and a second reset leg 232, is coupled in parallel with the capacitor 208. The first leg 228 is coupled to the ground 214. The control leg 230 is coupled, for example, to the third output 104 of the clock circuit 70. The second leg 232 is coupled to the output 216.

[0038] A hold switch 234, having a first hold leg 236, a hold control leg 238, and a second hold leg 240, is coupled between the second integration leg 222 and the ground 214. The first leg 236 is coupled to the second integration leg 222. The control leg 238 is coupled, for example, to the inverting output of the set/reset switch stated above. The second leg 240 is coupled to the ground 214.

[0039] The integration switch 206 is switched on by the rising edge of a clock pulse, allowing the current source 204 to charge the capacitor 210 and in effect integrating a constant current to generate a voltage ramp proportionally over time. When a subsequent data pulse arrives, the coordinating signal received by the integration control leg

220 toggles the integration switch 206 open, switching the integrator 200 into a hold mode by switch 234. Either switch 206 or switch 234 is in a closed state during the stated modes. During the hold mode voltage of the output terminal 216 may be read. When the reset switch 226 is closed the capacitor 208 is shorted to the ground 214, thereby resetting voltage of the output 216 to approximately zero.

[0040] Referring now to Figure 5, a detailed schematic diagram of a sample integrator 250 that correlates with the schematic of the integrator 200 in accordance with an embodiment of the present invention is shown. The integrator 250 includes seven transistors 252 and a buffer 254. Each transistor 252 has a respective emitter, base, and collector, which have associated numerical designators. The buffer 254 may be replaced with a differential buffer.

[0041] Collector and emitter legs of the first transistor 256, the second transistor 258, and the third transistor 260 are in series such that the first emitter 262 is coupled to the second collector 264 and the second emitter 266 is coupled to the third collector 268. The first collector 270 is coupled to the ground 272. A first resistor 274 is coupled

between the third emitter 276 and a voltage source 278. The first base 280 is coupled to a reset terminal 282. The second base 284 is coupled to an integration terminal 286. The third base 288 is coupled to a bias voltage source 290.

[0042] A first capacitor 292, having a negative terminal 294 and a positive terminal 296, is coupled between the first emitter 262 and the ground 272. The negative terminal 294 is coupled to the first emitter 262 and the positive terminal 296 is coupled to the ground 272.

[0043] Collector and emitter legs of the third transistor 260, the fourth transistor 298, and the fifth transistor 300 are also coupled in series such that the fourth emitter 302 is coupled to the fifth collector 304 and the fifth emitter 306 is coupled to the third collector 268. The fourth collector 308 is coupled to the ground 272. The fourth base 310 is coupled to the ground 272. The fifth base 312 is coupled to a hold terminal 314.

[0044] The sixth transistor 316 has a sixth collector 318 that is coupled to the ground 272 and a sixth emitter 320 that is coupled to a negative terminal 322 of a second capacitor 324. A positive terminal 326 of the second capacitor 324 is coupled to the ground 272. The sixth base 328 is cou-

pled to the reset terminal 282.

[0045] The seventh transistor 330 has a seventh collector 332 that is coupled to the negative terminal 322 and a seventh emitter 334 that is coupled to the third collector 268. A second resistor 336 is coupled between the seventh base 338 and the third collector 268.

[0046] The buffer 254 includes a non-inverting input 340, an inverting input 342, an output terminal 344, and an inverted output terminal 346. The non-inverting input 340 is coupled to the seventh collector 332. The inverting input 342 is coupled to the first emitter 262.

[0047] Referring now to Figures 4 and 5, the current source 204 is formed by the third transistor 260 and the first resistor 274. The bias voltage source 290 sets the amount of current flow through the third transistor 260. The second transistor 258 performs as the integration switch 206. The fifth transistor 300 performs as the hold switch 234. When the integration terminal 286 is high, representing reception of an integration signal, the current charges the first capacitor 292. When the integration terminal 286 is low, the current flows through the fourth transistor 298 and the fifth transistor 300, which is also when the output terminal 344 is read.

[0048] The buffer 254 cancels errors in the integration signal, such as parasitic errors. The seventh transistor 330 and the second capacitor 324 form a dummy voltage reference. The buffer 254 compares voltage across the first capacitor 292 with voltage of the dummy reference when generating an output signal, such as the resulting signal IntA. In comparing the voltage across the first capacitor 292 with the that of the dummy reference the buffer 254 cancels errors in the integration signal, since errors that are in the integration signal are also in the dummy reference.

[0049] After the output terminal 344 is read, the integrator 250 may be reset through use of the first transistor 256 and the sixth transistor 316 by pulsing the reset terminal 282 high.

[0050] Referring now to Figure 6, a logic flow diagram illustrating a method of extracting information from PPM signals in accordance with multiple embodiments of the present invention is shown. Although the method of Figure 6 is described with respect to the receiver 30 and the embodiment of Figure 2, it may be easily modified to apply to other receivers and embodiments of the present invention.

[0051] In step 350, the receiver 30 receives one or more PPM signals, such as the data signals 38, via the data receiver 34. The clock receiver 32 receives the reference clock signal 36 and the data receiver 34 receives the data signal 38, simultaneously.

[0052] In step 352, the transimpedance amplifiers 40 and 42 convert the clock signal 36 and the data signal 38 that are received in the form of current signals into voltage swing type signals.

[0053] In step 354, the timer circuits 54 and 56 widen the pulses of the converted clock signal 36 and the data signal 38. Duration of the clock signal 36 and the data signal 38 are increased, to ease and improve accuracy in detection of each pulse therein.

[0054] In step 356, the clock circuit 70 separates the clock signal 36 into the out-of-phase coordinating clock signals A, B, and C.

[0055] In step 358, the integrators 78 are clocked or gated to generate the time-integrated signals IntA, IntB, and IntC in response to the coordinating clock signals A, B, and C and the data signal 38. The integrators 78 begin integration of a constant current, set by the source 204, in response to the coordinating clock signals A, B, and C. The

integrators 78 cease integration in response to the data signal 38.

[0056] In step 360, the resulting demodulated signal V_{dem} is generated through the gating and summation of the time-integrated signals IntA, IntB, and IntC.

[0057] The above-described steps are meant to be an illustrative example; the steps may be performed sequentially, simul-taneously, synchronously or in a different order depend-ing upon the application.

[0058] The present invention provides a robust PPM receiver that is capable of receiving high data rates, has high signal resolution, and improved signal-to-noise performance.

[0059] While the invention has been described in connection with one or more embodiments, it is to be understood that the specific mechanisms and techniques which have been de-scribed are merely illustrative of the principles of the in-vention, numerous modifications may be made to the methods and apparatus described without departing from the spirit and scope of the invention as defined by the ap-pended claims.